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# Novel carrier functions based on CFD for fundamental fortification and improved harmonic profile for multilevel inverters

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## Abstract

*This paper carved out five novel carrier functions based on Control Freedom Degree (CFD) which is aimed at producing improved fundamental voltage with reduced THD and power loss over wide operating conditions. A pulse rotation unit using digital logic circuit is designed to rotate the proposed novel carrier PWM and fundamental switching signals to balance power loss among the H- Bridges in CHBMLI. The performance of the suggested carrier based PWM strategies are studied in Matlab/Simulink and a laboratory prototype is constituted to validate the simulated results. The study avails Xilinx Spartan 3E FPGA controller for generating PWM signals from the suggested novel carriers to drive the 7- level CHBMLI for generating 7- level output voltage.*

Keywords: *Novel Carrier functions, amalgamated carrier PWM, CHBMLI, FPGA*

## 1. INTRODUCTION

Multilevel Voltage Source Inverters (MLVSIs) are favored over conventional three-level inverters due to their ability to produce output voltages in finer steps, leading to significantly reduced distortion. They also offer benefits such as minimized voltage and current stress, low-distortion input current, reduced common-mode voltage, and effective operation even at lower switching frequencies. Among the various control strategies, Carrier-Based Pulse Width Modulation (CPWM) remains a fundamental technique in managing Multilevel Inverters (MLIs), particularly for high-power scenarios where enhanced power quality and lower harmonic content are essential. The primary CPWM approaches—Level-Shifted (LS-PWM), Phase-Shifted (PS-PWM), and Phase Disposition (PD-PWM)—have evolved over time [1–7] to cope with emerging challenges such as complex inverter topologies, unequal DC-link voltages, loss minimization, and seamless integration with renewable energy systems. To improve harmonic performance in 5-level Cascaded H-Bridge (CHB) inverters**,** Biswas et al. proposed a novel modulation scheme termed Third-Harmonic Injected Inverted Sinusoidal Carrier PWM (THI2SCPWM). Designed specifically for induction motor drives, this technique integrates a third-harmonic signal into an inverted carrier waveform. As a result, it achieves lower Total Harmonic Distortion (THD) and minimizes torque ripple, especially when paired with a 36-pulse AC-DC converter interface, demonstrating its suitability for industrial-grade motor drive applications [8]. In response to the complexities presented by Asymmetric Cascaded H-Bridge (ACHB) multilevel inverters**,** Zhang et al. introduced the Asymmetric Selected Harmonic Mitigation PWM (ASHM-PWM) approach, which effectively addresses power balancing and harmonic mitigation in systems with uneven voltage sources.

This method applies particle swarm optimization to select switching angles that achieve harmonic mitigation while balancing power among cells with different DC-link levels. The result is reduced output



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voltage THD and improved power distribution in complex asymmetric topologies, a critical factor for modular and scalable inverter architectures [9]. This synergy between carrier PWM and computational intelligence markedly advances control precision and reliability.

The operational efficiency of carrier PWM in modular inverter variants, such as quasi-impedance source inverters (qZSI), has also seen improvement. Rahman et al. proposed a hybrid Phase-Opposition Disposition And Phase-Shifted (PODPS-PWM) technique, reducing switching losses by more than 39% compared to conventional PS-PWM. This approach further enhances power extraction under partial shading in photovoltaic applications by allowing unequal power distribution among modules, thus improving both harmonic performance and system efficiency [10]. Such hybrid carrier PWM developments exemplify adaptations for modern energy systems requiring both power quality and loss optimization.

Scaling hardware complexity and control sophistication, Juarez-Abad et al. demonstrated FPGA implementations of conventional LS-PWM and hybrid PWM on Binary-Asymmetric Cascade Multilevel Inverters (B-ACMLI). Utilizing floating-point arithmetic within FPGA architectures supports real-time, high-precision switching control, reducing resource consumption and power demand while improving switching speed. This hardware-software co-design advances the practical deployment of carrier PWM schemes in asymmetric and modular inverter designs [11].

Theoretical and algorithmic advancements complement practical implementations. Nho and Youn introduced a unified mathematical framework for multiple carrier-based PWM strategies across diode-clamped and cascaded topologies, enabling explicit independent control over fundamental voltage components and redundant vectors. This comprehensive formulation bridges the gap between carrier-based and space vector PWM methods, ensuring theoretically optimal modulation with reduced harmonics [12]. Similarly, Kim et al. extended carrier PWM to multilevel four-leg voltage-source inverters, introducing offset voltages optimizing switching sequences to minimize harmonics even for unbalanced or nonlinear loading conditions [13]. These fundamental studies underpin the accuracy and robustness of carrier PWM control.

Hybrid PWM approaches further enhance modulation performance for MLIs. Ye et al. proposed a hybrid multi carrier PWM combining the advantages of Carrier Phase Shift (CPS) and carrier disposition methods, achieving natural power balance among CHB cells alongside improved harmonic spectra. Simulation and experimental results confirm that such carrier reconstruction techniques optimize the trade-offs between harmonic reduction and power sharing [14]. This direction is significant for complex inverter systems where harmonics and power losses must be simultaneously minimized.

In medium-voltage motor drives, carrier-based modular multilevel inverters employing PWM have demonstrated excellent voltage quality and robustness. Hagiwara et al. presented a modular multilevel PWM inverter featuring cascaded bidirectional chopper cells with PWM control, highlighting voltage fluctuation analysis crucial for reliable motor operation at medium voltages [15]. Although earlier than 2021, this work remains a vital reference for understanding carrier PWM in industrial scale MLIs.

Further research also explores carrier PWM strategies to support voltage balancing. Vahedi et al. designed a cascaded inverter structure employing multicarrier PWM to ensure capacitor voltage balancing even under unequal DC sources, which is essential for stable and efficient multilevel inverter operation, particularly in renewable energy contexts [16].


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Collectively, the recent research contributions underscore a sustained research trajectory where carrier PWM techniques for MLIs are evolving through hybrid modulation schemes, optimized harmonic mitigation, switching loss reduction, and real-time digital implementations. The integration of computational intelligence, mathematical modeling, and FPGA-based control is enhancing the precision and adaptability of carrier PWM, making it more viable for complex, asymmetric and renewable-integrated inverter topologies. These advancements contribute fundamentally to improving power quality, efficiency and reliability in modern power electronic systems.

This paper suggests five novel carrier functions suitable for CHBMLI with a motivation to improve fundamental output voltage and to equalize the switching losses among the power devices within the cell and among the H- bridge cells.

## 2.**Review of Multicarrier PWM strategies**

There are various control strategies available for Multilevel Inverters (MLIs) aimed at generating stepped output voltages with minimized harmonic distortion. One widely known technique, introduced by Carrara et al. [1], is the **Multicarrier Pulse Width Modulation (MCPWM)**, which utilizes high-frequency carrier signals. These carriers are arranged vertically to distinguish between different disposition techniques such as **Phase Disposition (PD), Alternative Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD), Phase Shifted Carrier (PSC),** and **Carrier Polarity Variation (CPV)**. n MCPWM, a single reference sine wave is compared with a set of triangular carriers arranged near the zero axis, producing distinct switching pulses for each output voltage level. Among the techniques, **PD** places all carrier signals in phase, as shown in Fig. 1. In **POD**, carriers above and below the reference axis remain in phase within their groups, but the two groups are shifted by 180° from each other (Fig. 2). **APOD** arranges carriers so that adjacent ones are in opposite phases (Fig. 3), whereas **CPV** introduces random polarity variations within each carrier band (Fig. 4). These carrier disposition methods have shown noticeable improvements in **Total Harmonic Distortion (THD)** and have reduced switching losses under constant output conditions. Among them, **PD** often delivers superior harmonic performance [3]. In the **PSC** method, carrier signals are phase-shifted horizontally to mitigate additional harmonic sidebands (Fig. 5) [7]. A modified approach by Steinke involves augmenting the reference sine wave with a zero-sequence component, allowing a 15% increase in modulation index before entering the over-modulation region. Additionally, **Tolbert et al.** proposed the **Variable Frequency Carrier Band (VFCB)** method, which controls the switching events at each level by estimating the duration the reference signal stays within specific carrier time bands (Fig. 6) [7].

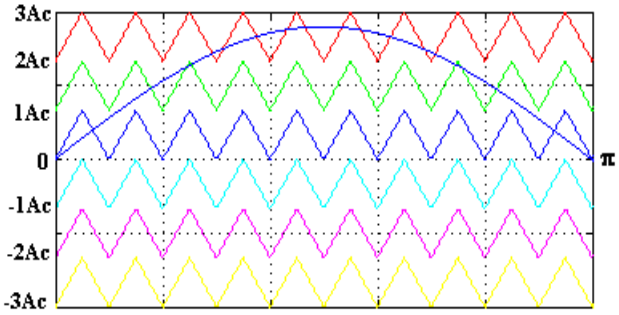


**Fig. 1** PD


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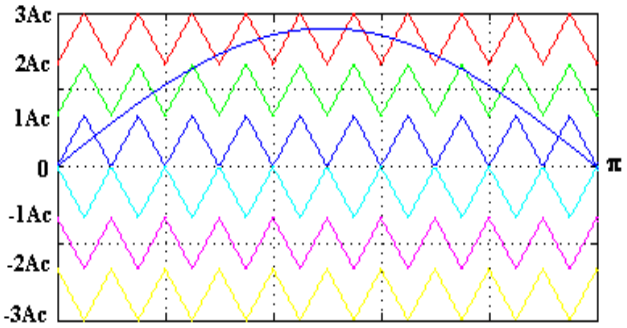


**Fig. 2** POD

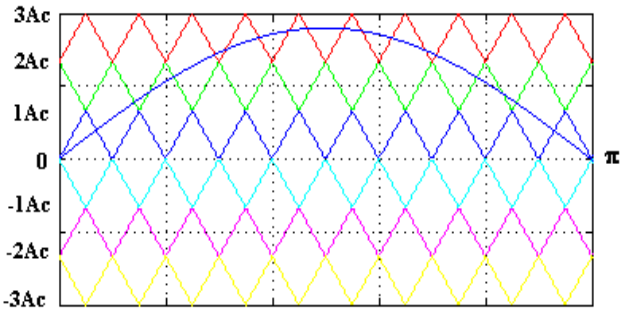


**Fig. 3** APOD

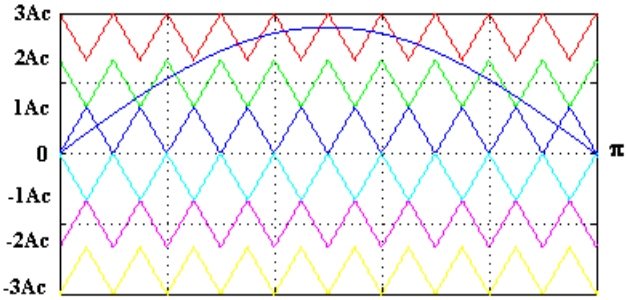


**Fig. 4** CPV

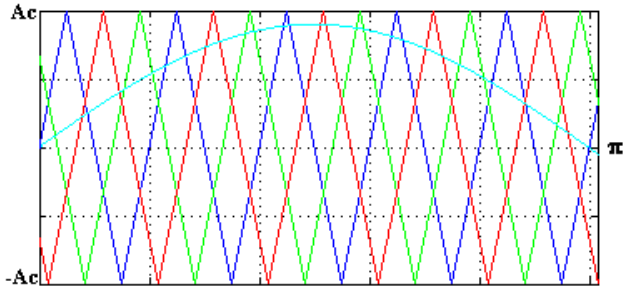


**Fig. 5** PSC


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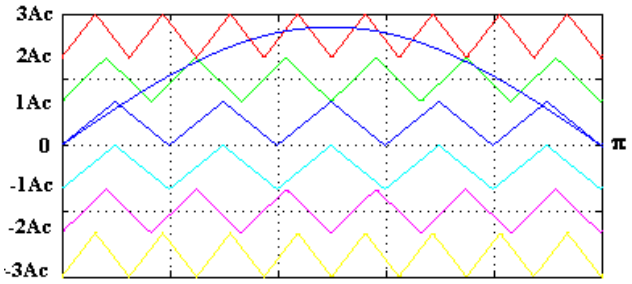


**Fig. 6** VFCB

### 3.Novel Submissions Based on CFD

MLI have Control Freedom Degrees (CFD) on carrier and reference functions that can be used to modulate the output voltage. With reference to the type and position of the carrier in the band as mentioned in the above section, the carrier signals have more novel functions based on CFD. Similarly apart from basic sine reference signal, the modulating signal has also significant modification based on CFD through addition or injection of harmonic voltage to harness maximum dc-link voltage and expand its linearity over the entire operating region.

### A. CFD on Carrier

### (i) M to W and W to M Carrier

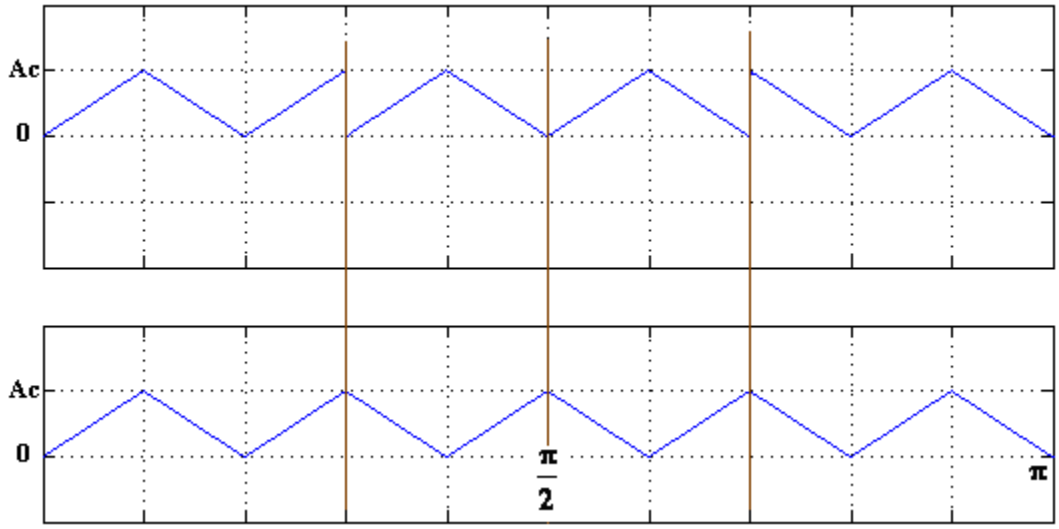


**Fig. 7** W to M type conversion


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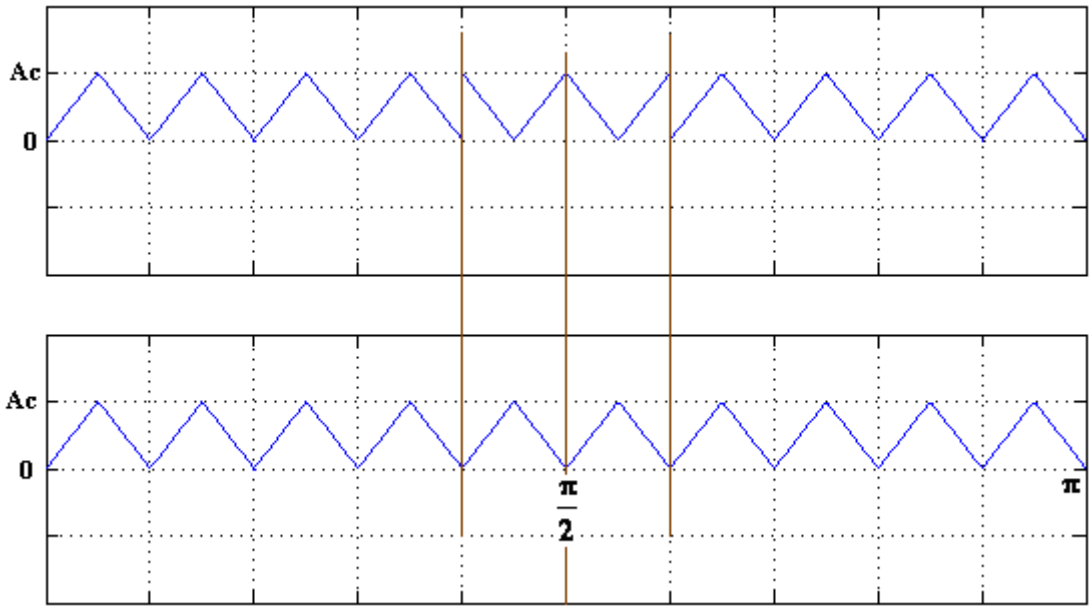


**Fig. 8** M to W type conversion

The triangular carrier is modified by combining two neighbouring triangles of carrier wave around the apex region of the sine reference and doing a phase shift keying for 180º resulting W or M shape and widens the width of the pulses near the apex region of reference sine signal to enhance the fundamental output voltage and better THD. [17]. Fig. 7 shows the conversion principle for W to M and M to W in Fig. 8 respectively. It is seen that W to M conversion is possible only for (odd $M_f$) while M to W conversion is applicable for (even $M_f$) per half cycle of reference waveform. As a result of this, the modified segment in the carrier signal has more number of pulses but the remaining portions remains unaffected.

**(ii) Inverted sine carrier**

A high frequency sine wave is rectified by precision rectifier and inverted by an inverting amplifier to produce inverted sine wave as shown in Fig. 9. For a given ($M_f$), the area under the high frequency inverted sine wave is more than classical triangle carrier results higher output voltage [18].

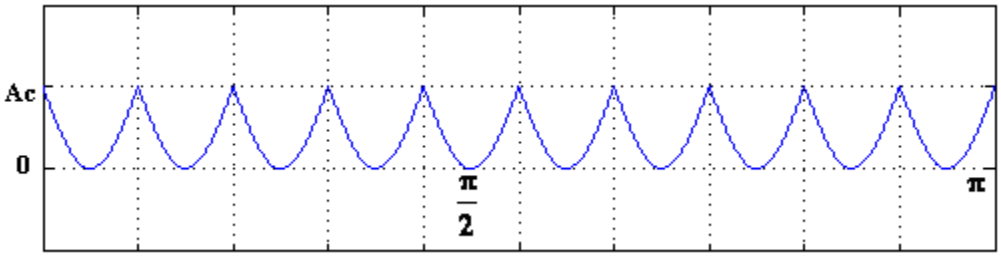


**Fig. 9** Inverted sine carrier

**(iii) 60˚ PWM**


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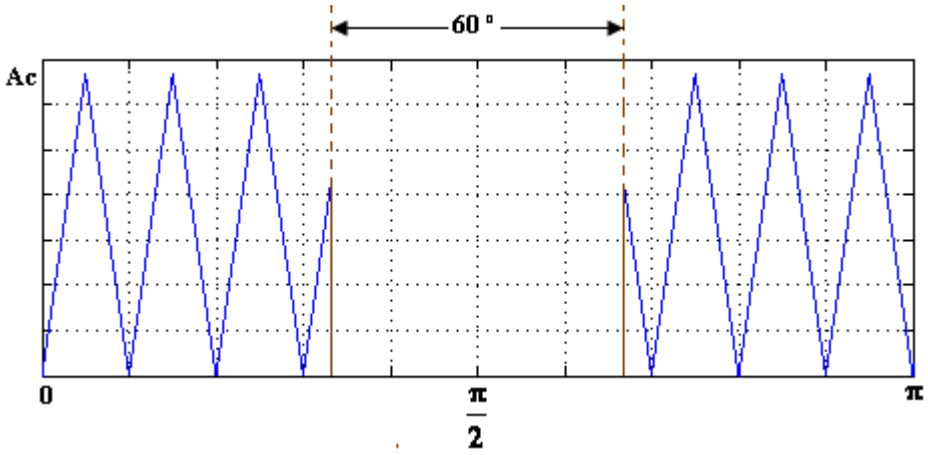


**Fig. 10** 60° PWM

The width of the pulse does not vary appreciably near the apex region of reference sine wave over a range of ($M_a$) [19]. This paves the way of modifying the carrier wave leaving empty band of 30º on either side near apex region of the reference sine wave as shown in Fig. 10. This will bring pulse dropping over 60º near apex region of the modulating sine producing enhanced output voltage and improved harmonic distortion compared with traditional triangle carrier PWM. It further reduces the number of switching applied to power devices and hence switching losses.

**(vi)Clubbed inverted sine carrier**

This technique is an enhancement of the 60° PWM strategy, aiming to minimize total harmonic distortion (THD) by integrating an inverted sine carrier waveform into the central portion of the modulation signal. As illustrated in Fig. 11, the modified carrier pattern significantly boosts the fundamental output voltage. It employs the same reference signal used in conventional PWM to produce the required pulse signals. The peak region of the output pulses scales proportionally with the corresponding area of the inverted sine section. This approach results in a higher fundamental voltage component along with an improved harmonic spectrum.

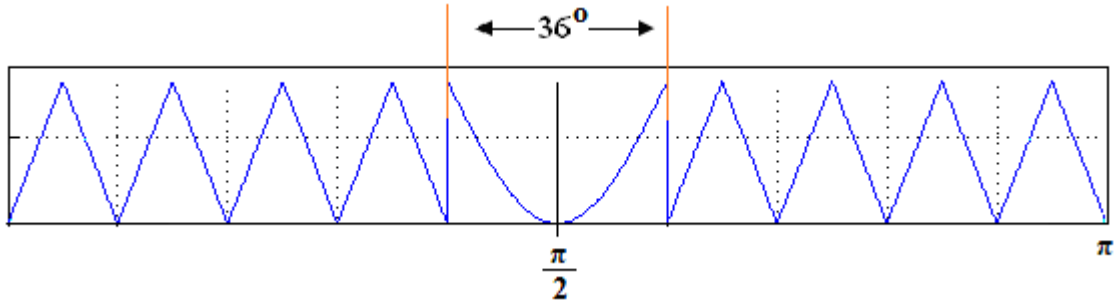


**Fig. 11** Clubbed inverted sine carrier

**(V) Variable amplitude triangle carrier**

In this method, the amplitude of the high-frequency triangular carrier waveform is dynamically adjusted over each half-cycle of the output voltage based on the instantaneous magnitude of the normalized reference sine wave [20]. Compared to the conventional carrier, the adjusted waveform results in broader pulse widths for the same modulation index (Mf), thereby enhancing the output voltage and lowering the


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total harmonic distortion (THD), all while avoiding the onset of overmodulation. The corresponding waveform is illustrated in Fig. 12.

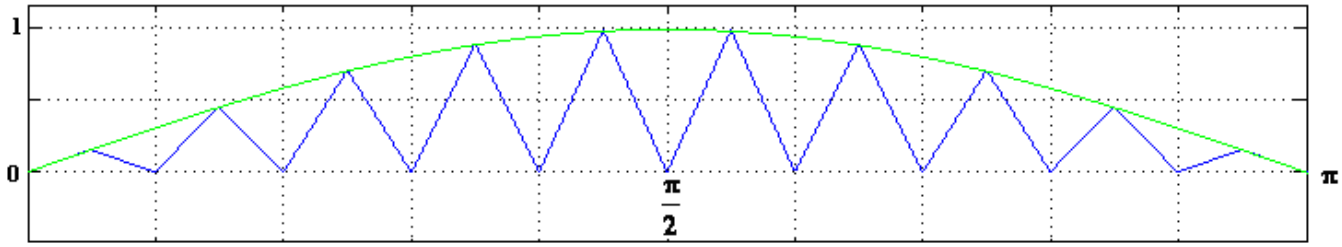


**Fig. 12** Variable amplitude triangle carrier

### B.CFD on reference function

It is evident from the past literatures that the fundamental component in the PWM output voltage is smaller than fundamental frequency switching operation. The ratio of fundamental output voltage to dc-link utilization is higher in fundamental frequency switching method. This indicates that the conventional modulating signal required a modification based on CFD to extend the output voltage linearity effectively. There is a possibility of adding zero sequence component of third harmonic wave to fundamental reference sine wave that makes more dc link utilization and improved harmonic performances.

### (i) Third harmonic injected reference

The third harmonic sine wave is injected to the fundamental frequency reference so as to increase the amplitude of the fundamental component. A third harmonic wave is added to reference sine wave is shown in Fig. 13. The analytical expression to find the optimum value of third harmonic to be added to the reference sine wave is given in below equation.

$$Y(t) = 1.155(\sin\omega t + (1/6)\sin 3\omega t)$$

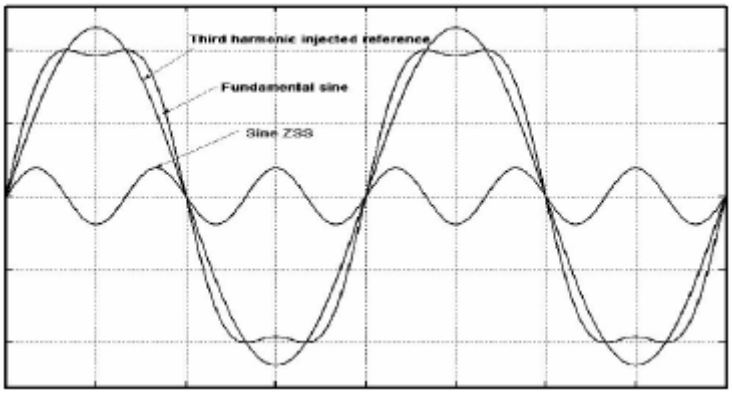


**Fig. 13** Third harmonic injected reference

### (ii) Triplen harmonic injected reference


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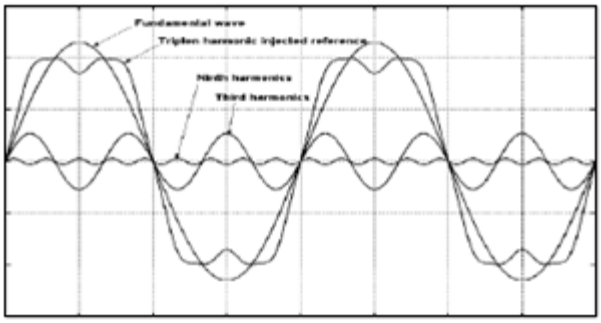


**Fig. 14** Triplen harmonic injected reference

This technique is an extension of the third harmonic injection method, where the reference signal is modified by incorporating harmonics that are integer multiples of three. These additional components enhance the modulating waveform, as depicted in Fig. 14. The resulting analytical expression for the modified reference signal is: **$Y(t) = 1.15\sin\omega t + 0.27\sin 3\omega t - 0.029\sin 9\omega t$**

**4.Pulse rotation unit using digital logic circuit**

A **randomized switching mechanism** has been incorporated into the PWM strategy to mitigate imbalanced switching losses and uneven thermal distribution across the semiconductor devices. The proposed **pulse rotation framework** alternates between **Fundamental Switching (FS)** and **Multicarrier PWM (MPWM)** signals across multiple output cycles, ensuring more uniform stress distribution among the switching components [21]. This hybrid control method combines the **loss-minimizing advantages** of FS with the **harmonic enhancement** capabilities of MPWM.

In this approach, each power switch operates in a **sequential frequency mode**, meaning two of the four switches in an inverter leg function at lower switching frequencies, while the other two operate at higher frequencies, replicating the performance of MCPWM. A **PWM rotation logic circuit** is integrated with a sequence-based switching controller to evenly distribute power loss across all modules. The system architecture, outlined in Fig. 16, includes a **PWM signal generator**, **random signal source**, **randomized switching logic (RMC)**, and a **PWM redistribution controller**.

Fig. 16(a) illustrates the schematic for the PWM signal generator assigned to a single inverter module. The signal (A')—a randomized logic output—is produced using a D-type flip-flop, as shown in Fig. 16(b). Inputs to this flip-flop include:

- A square wave signal (A) with a frequency at half the fundamental value and 50% duty cycle,
- A synchronously toggled square wave signal (B), aligned with the positive and negative cycles of the reference sine wave, acting as the clock.

Since signal (A) has a frequency neither equal to nor a harmonic of the fundamental frequency, it facilitates generation of a random binary output (A'). In the setup depicted in Fig. 16(c), the PWM comparator (signal C) uses either rectified or modified reference waveforms in conjunction with a high-frequency triangular carrier (also potentially modified) to produce the modulation signal.

Depending on the state of A', switches S1 and S2 may operate at low frequency while S3 and S4 run at high frequency, or vice versa. This ensures that across time, all switches experience an **averaged switching frequency**, leading to a **balanced thermal load**.


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The **PWM redistribution controller**, implemented using another D flip-flop, dynamically rotates PWM patterns among different inverter modules. After every two fundamental cycles, the switching sequence is shifted—such that the PWM assigned to the first module is reassigned to the second, and so on, completing the cycle. This systematic rotation equalizes both voltage and current stress across all devices. Consequently, **identical power semiconductors and uniform cooling solutions** can be employed, simplifying the hardware design.

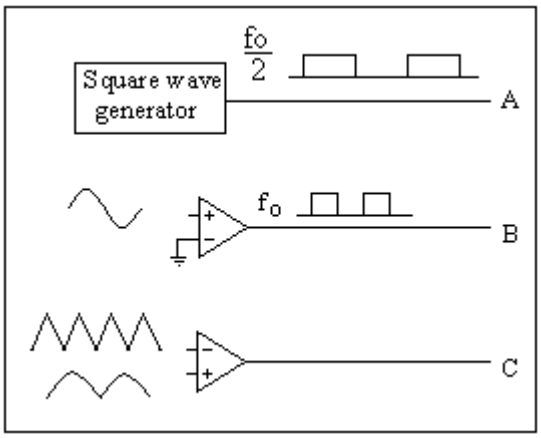


**Fig. 16 (a)** Base PWM generator

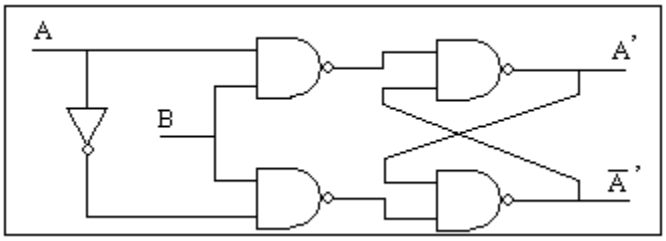


**Fig. 16 (b)** Random signal generator

## 5.Simulation and experimental Study

The performance evaluation of the proposed carrier strategies are studied for a 7- level CHBMLI shown in Fig. 17 using Matlab/Simulink R2021a with simulation parameters of step input voltage of 100V, carrier frequency ($f_c$) of 2kHz for W to M and 1 kHz for M to W carrier, inverted sine carrier, 60º carrier, clubbed sine carrier and reference frequency ($f_r$) = 50Hz respectively. The output voltage and harmonic spectra of five different modulators are shown in Figs. 18, 19, 20, 21, 22, 23, 24 and 25 respectively. The experimental prototype for the 7- level CHBMLI has been developed using (IRG4BC20SD) IGBTs and IR 2110 fate driver units for the same simulation specifications. A VHDL coding is used to generate the carrier signals in FPGA through Look up Table (LuTs) method and the PWM pulses are generated by comparing the modified carrier signals with reference sine wave. Figs. 30 and 31 represent the experimental test set up and output voltage along with harmonic spectrum for 60º PWM method.


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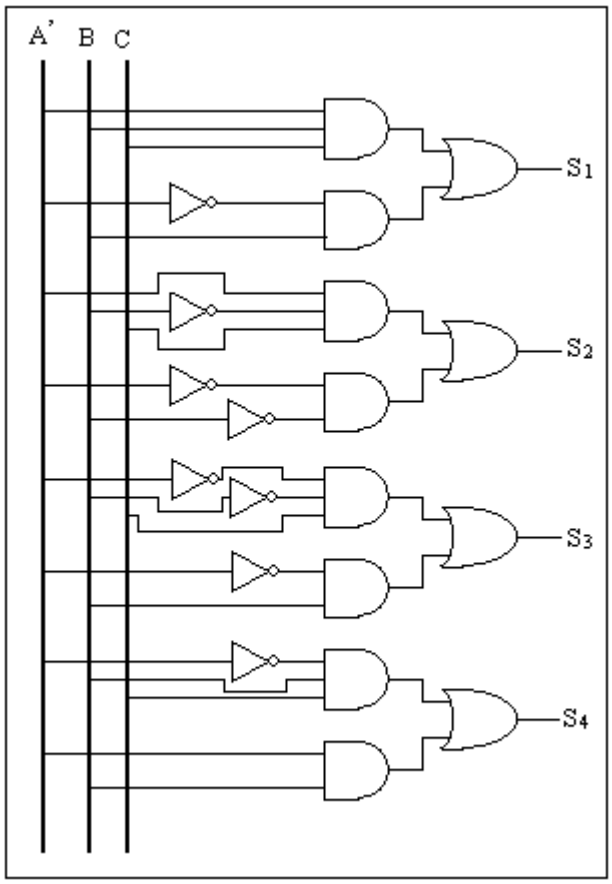


**Fig. 16 (c)** Random Switching controller

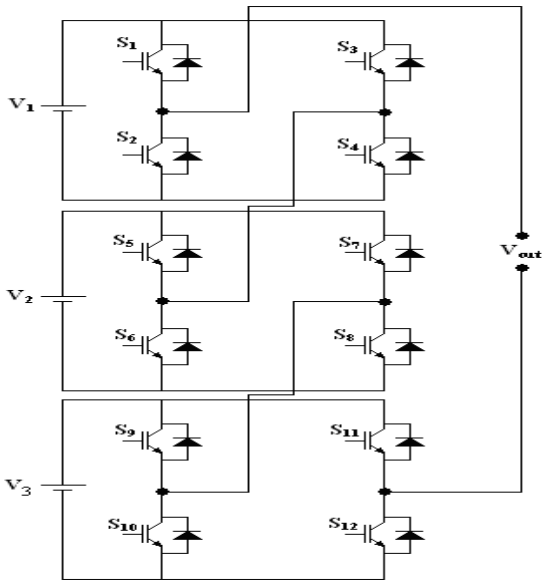


**Fig. 17** single phase seven level cascaded MLI


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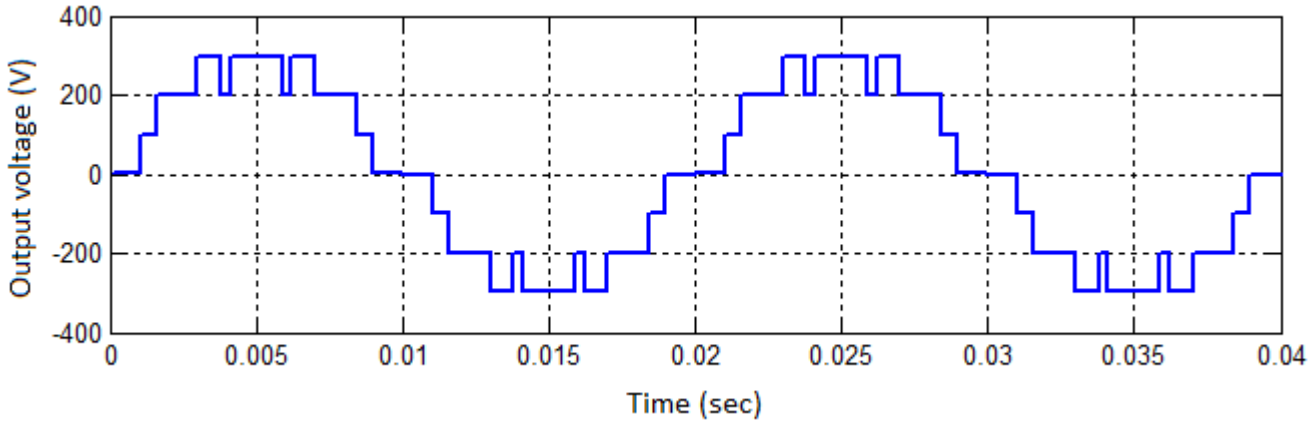


**Fig. 18** Output voltage waveform- W to M

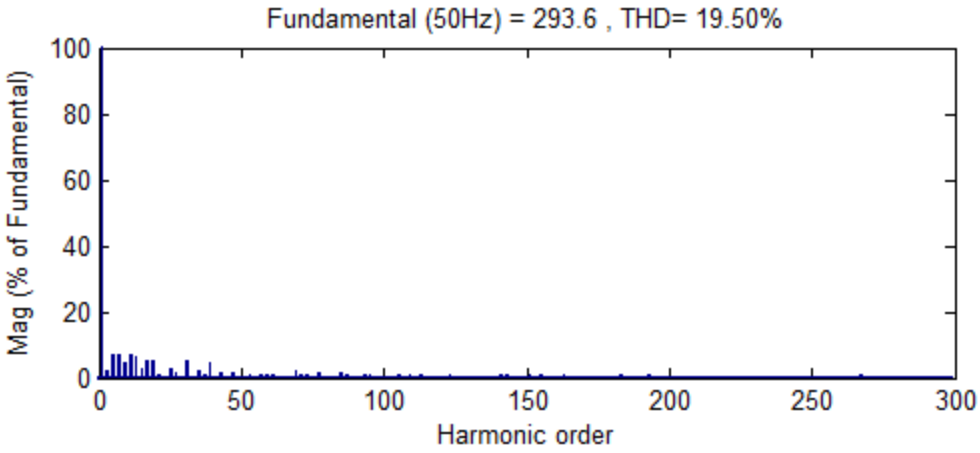


**Fig. 19** Output voltage spectrum- W to M

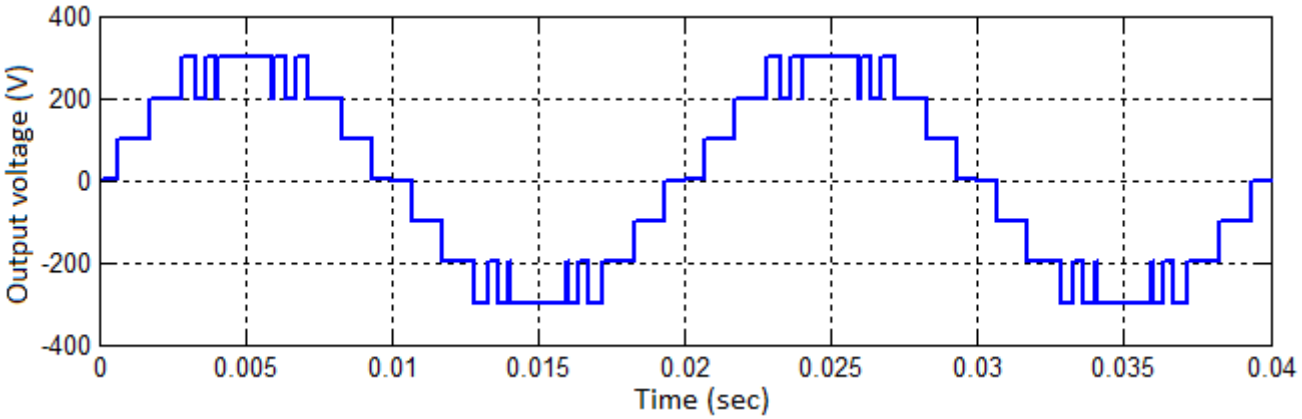


**Fig. 20** Output voltage waveform- M to W


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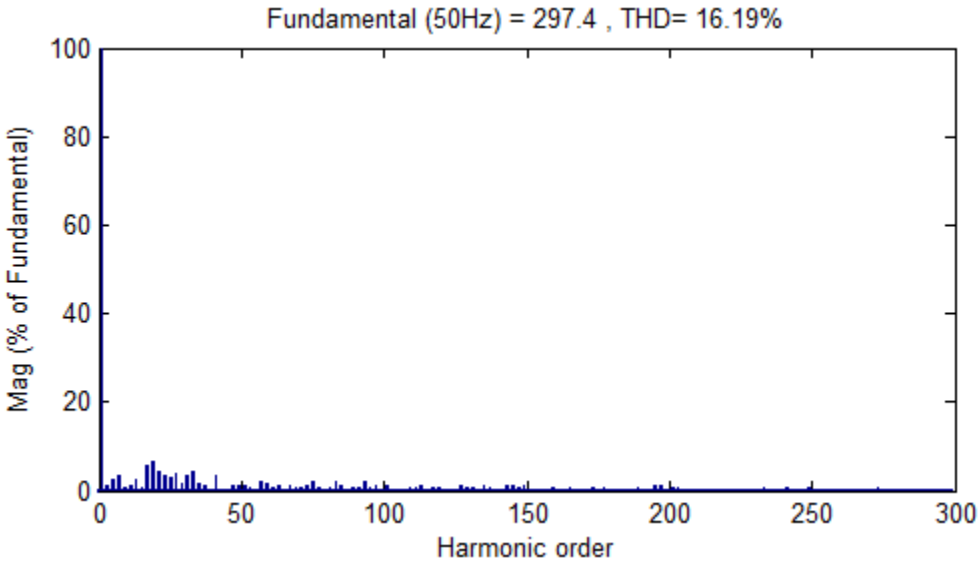


**Fig. 21** Output voltage spectrum- M to W

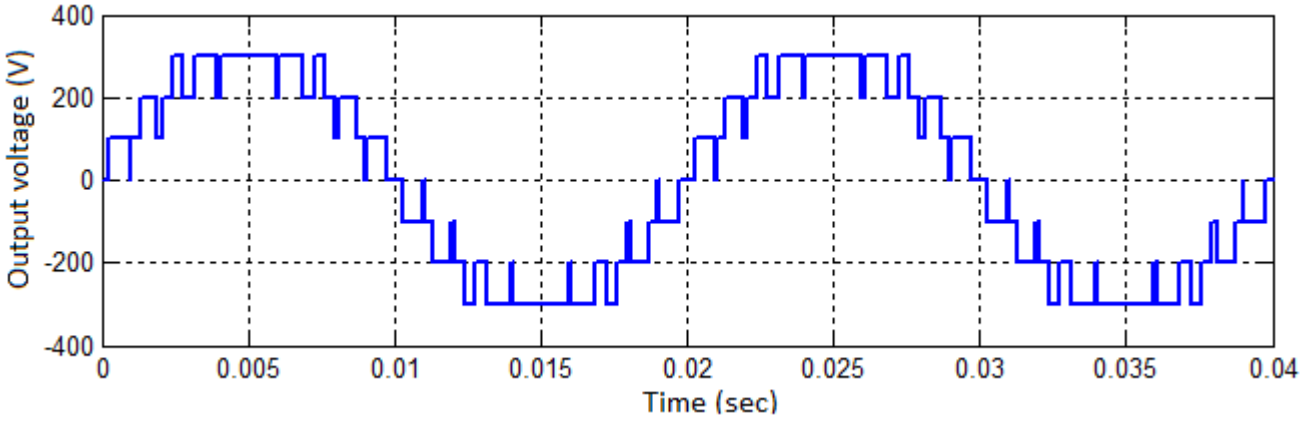


**Fig. 22** Output voltage waveform- ISCPWM

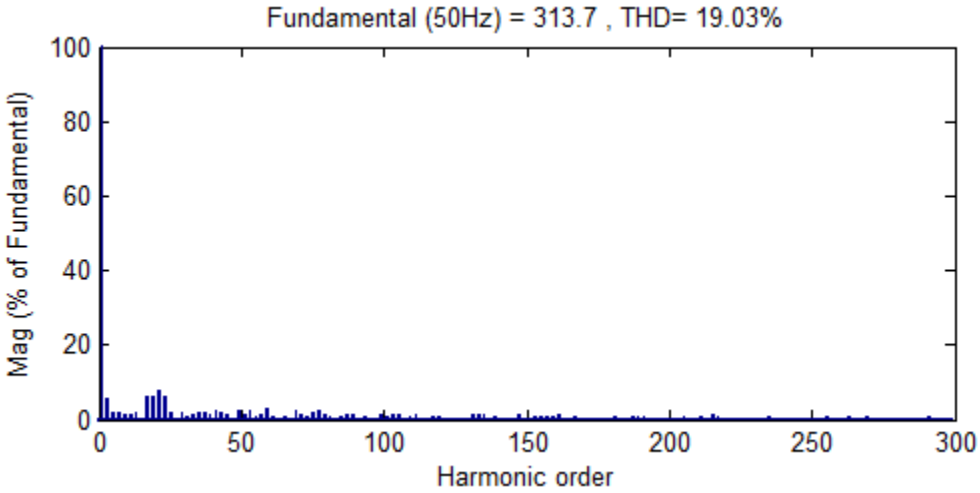



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**Fig. 23** Output voltage spectrum- ISCPWM

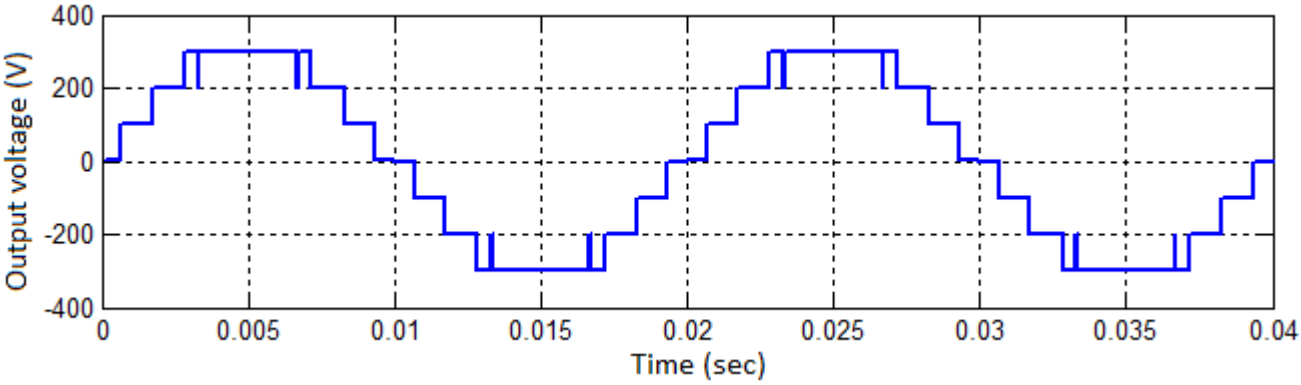


**Fig. 24** Output voltage waveform- 60º Carrier PWM

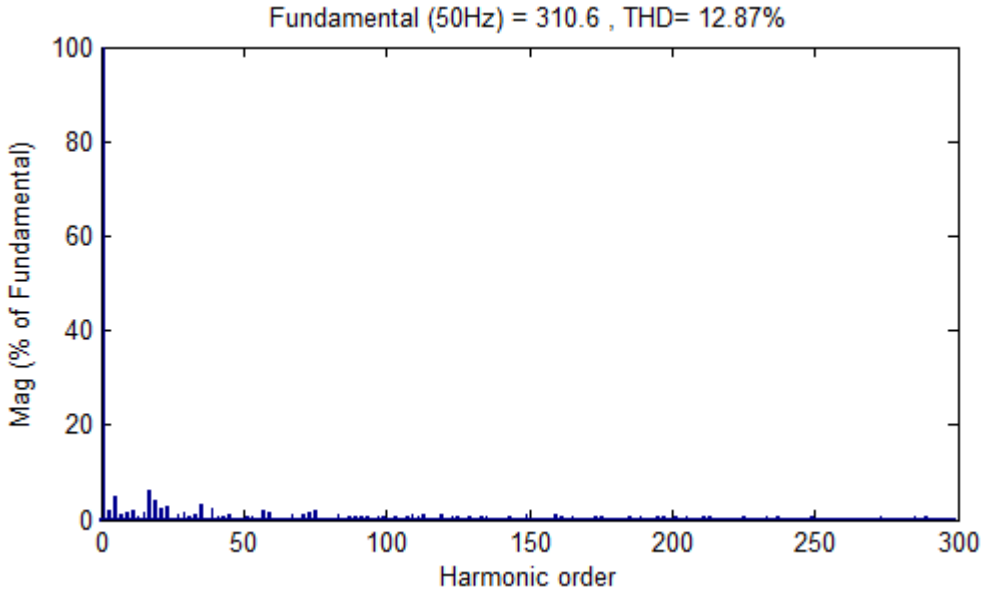


**Fig. 25** Output voltage spectrum- 60º Carrier PWM

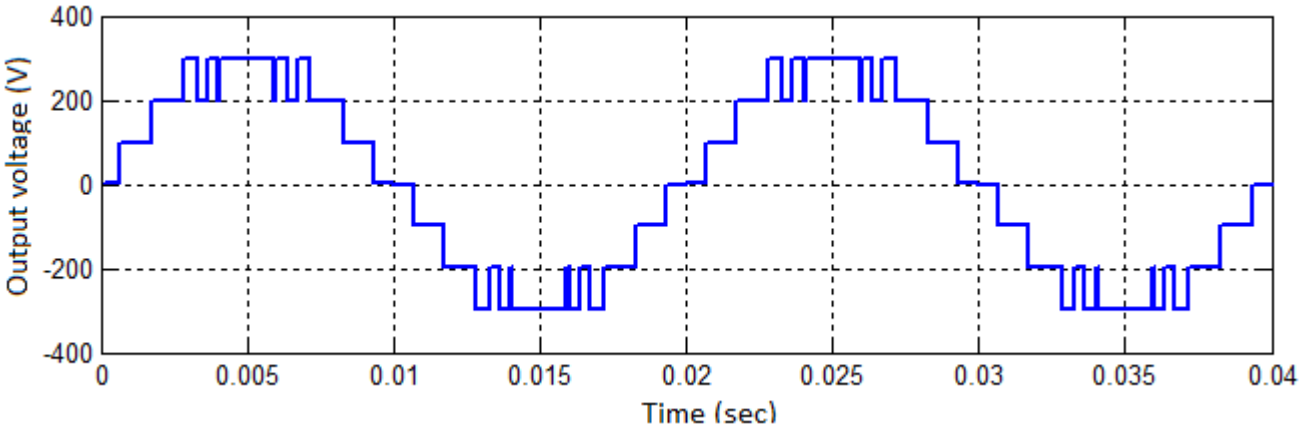



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**Fig. 26** Output voltage waveform- CSCPWM

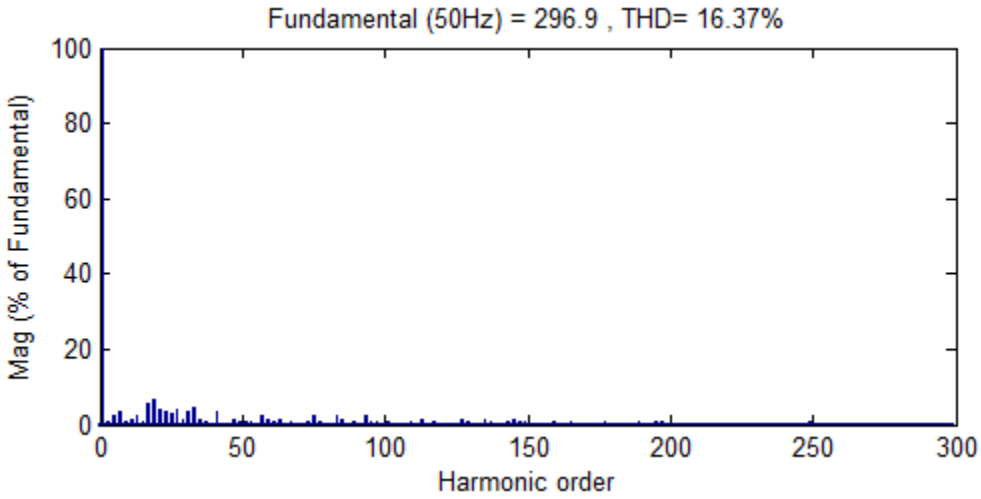


**Fig. 27** Output voltage spectrum- CSCPWM

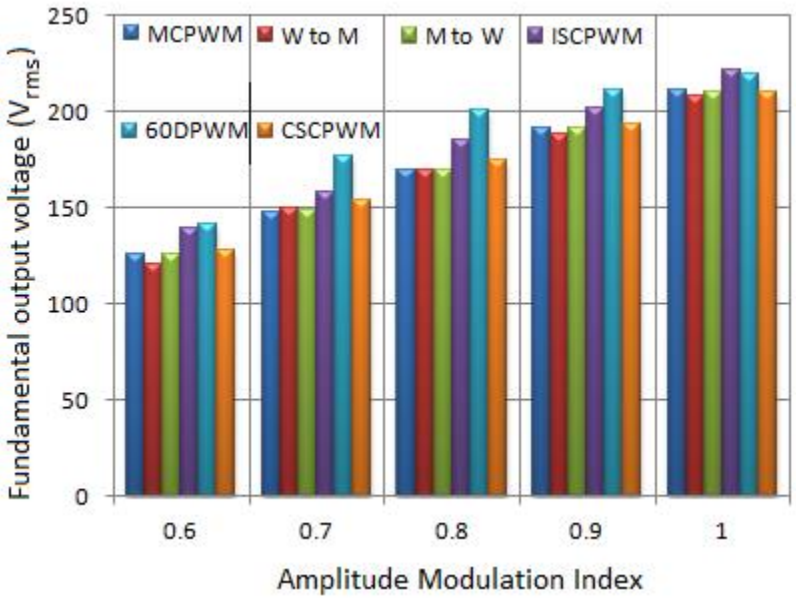


**Fig. 28** Variation of Fundamental output voltage against modulation depth


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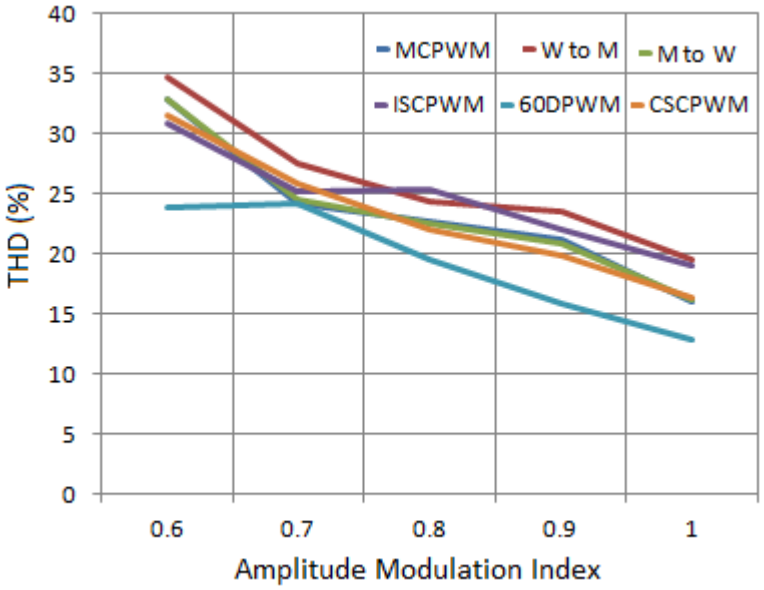


**Fig. 29** Variation of THD against Modulation depth

The variation of fundamental output voltage against modulation depth is presented in Fig. 28 between the conventional MCPWM and modified carrier PWM methods. It is seen that the 60º PWM propels higher out voltage over the entire operating range compared with MCPWM method, while the ISCPWM method gives slightly lower voltage value in par with 60º PWM. Between ISCPWM and 60º PWM methods, the width of the pulse near the apex region is constant in 60º PWM due to un-modulated segment from 60º to 120º and in ISCPWM the pulse width varies linearly with area of the inverted sine under the same segments. From the modulation index greater than 70%, MCPWM, W to M and M to W carrier PWM methods shows marginal variation in the output voltage for the same switching frequency. The carrier conversion takes place in the middle band of the carrier cycle and the remaining portion gets unaffected which results same pulses in the unaffected segments in the modified carrier PWM as that of MCPWM. The clubbed sine carrier gives the output voltage in par with M to W carrier due to the inclusion of inverted sine carrier in the un-modulated portion of 60º PWM method. Fig. 29 portrays the variation of THD as a function of modulation depth. It is to be noted that 60º PWM has lower THD compared with other methods.


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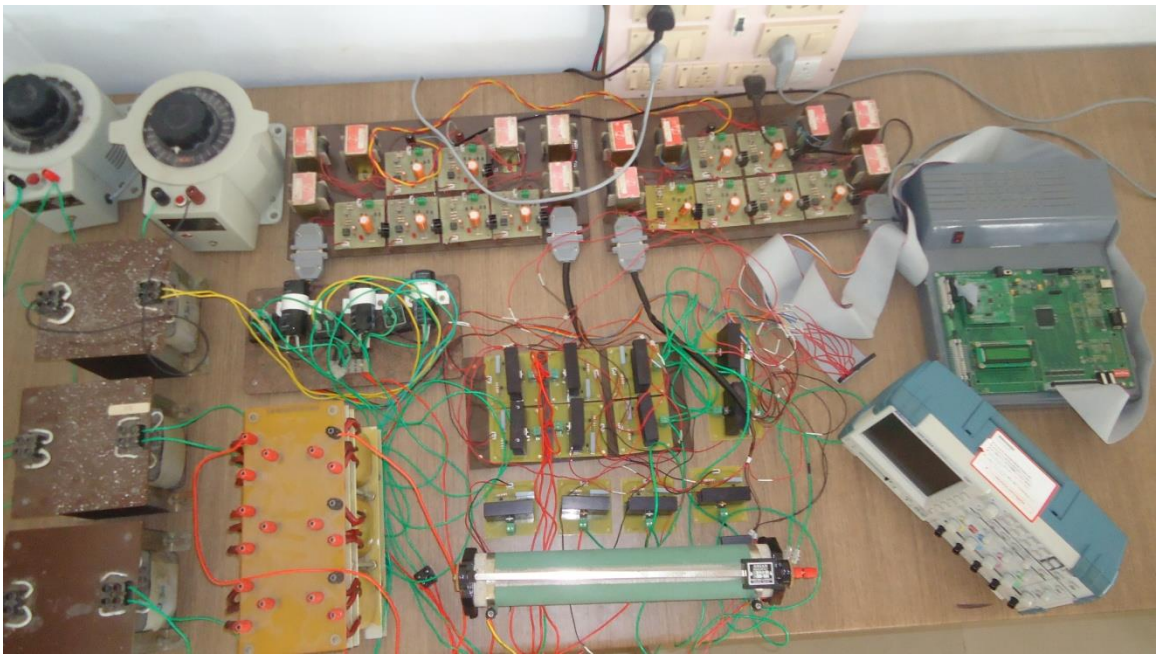
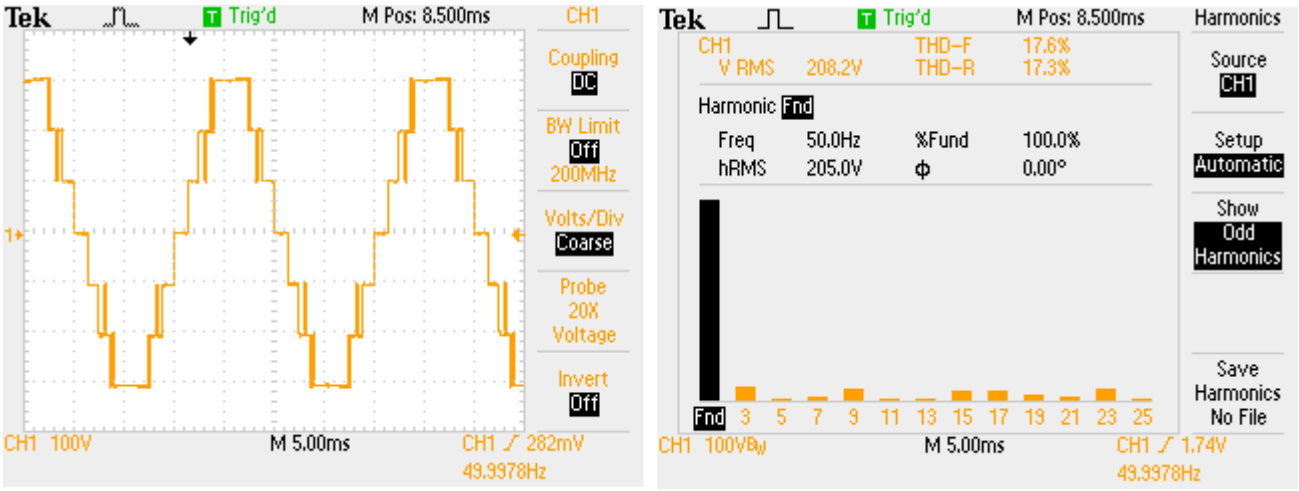


**Fig. 30** Experimental set up for 7- level CHBMLI




(a) (b)

**Fig. 31** (a) Output voltage (b) Voltage spectrum for 60º PWM

## 6.Conclusion

The proposed modified carrier PWM strategies influences in improving the fundamental output voltage by widening the width of the pulses in the pulse train over the entire modulation depth with lower THD. The suggested modified carriers have distinct characteristics in generating the output voltage and harmonic profile. It is observed from the simulation study that the W to M and M to W carrier PWM shows a marginal variation in the load profile compared with traditional PWM. On the other hand, the methods like ISCPWM, Clubbed sine carrier PWM and 60º PWM shows a large variation in the load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voltage for a given modulation depth and also in terms of THD. The experimental investigation echoes the merit of the modified carrier PWM suitable for industrial drive applications.

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