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DESIGN OF VGA CONTROLLER USING FIELD PROGRAMMABLE GATE ARRAYS

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ABSTRACT
VGA is a standard interface that is used in a variety of applications such as surveillance systems, ATM machines and video conferencing. VGA is used to link a computer to a monitor. The paper shows how to display a VGA monitor using the Xilinx platform and Verilog code. VGA timing is generated in this work, and its position and even size can be adjusted. To obtain the bit stream for FPGA implementation, the code is synthesised and a netlist is generated. There are five active signals in a VGA video transmission. R, G, B, H sync, V sync All other colours are created by modifying the three RGB signals. To validate the design, the RTL is obtained and simulation results are shown.

Keywords: VGA, RGB, DB-15 Connector, RTL

I. INTRODUCTION
VGA is a widely used standard interface in video surveillance and conferencing, as well as video players and payment vending machines. A monitor is attached to this system in order to display photos and information. The display's quality is primarily determined by the application's requirements. In AV equipment, there is a VGA connector, which is generally connected to a PC or laptop. This connector normally accepts an RGB signal from a linked device; this is usually the signal that is stimulated from the system, and it is compatible with both standard and high-definition resolutions.Its working principle is similar to that of a cathode ray tube, in which the picture is built one line at a time, starting from the top, and each line is displayed from left to right; in reality, this is accomplished by an electron beam directed from electromagnets within the screen that hits the pixels. R, G, B, H sync, and V sync are the five active signals in a normal VGA video stream, and by altering the RGB signals, numerous additional colours can be obtained. Figure 1 depicts a typical block diagram of a VGA controller.

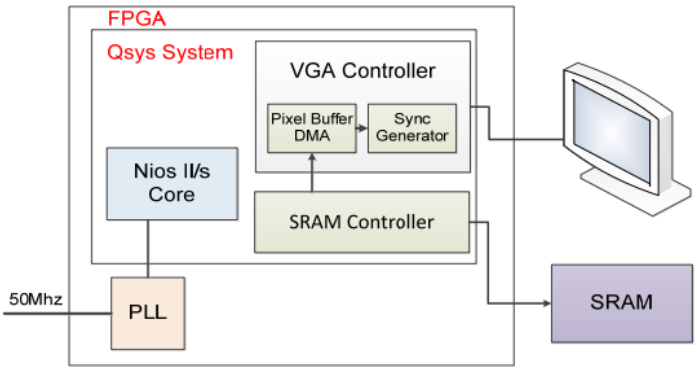

Figure 1 Block Diagram of VGA Controller

VGA connectors (D-SUB) are a set of plugs and sockets commonly used in older computer and communication applications. Its interface is a 15-pin plug and socket known as "D- connectors." Figure 2 depicts a common DB-15 connector schematic. It comes in 9, 15, 25, 37, and 50 pin versions.

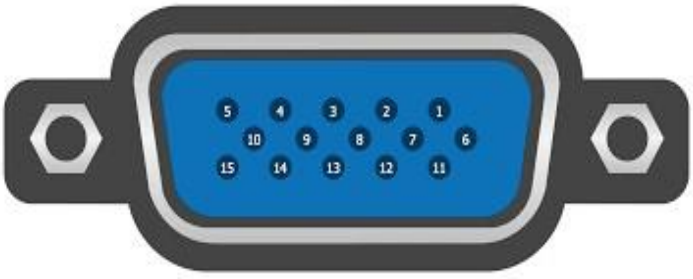

Figure 2 DB-15 Connector Schematic

Table 1. Pin Description of DB-15 Connector

ISSN 2394 - 9554

Pin Number	Description
1	Red
2	Green
3	Blue
13	Horizontal Sync
14	Vertical Sync
6,7,8,10,11	GND
4,5,9,12,15	No Connection

II. VGA SIGNAL DESCRIPTION

VGA is a three row 15 pin connector equipped with screw type locking mechanism. It transmits analog component of RGBHV video signal and DDC data. Signal loss is dominant as the length of the wire is enhanced. A typical video signal attained VGA connector comprises of the following five components: (i) Horizontal sync: digital signal, that scans a row,(ii)Vertical sync: digital signal, that scans an entire frame, (iii) Red (R): Analog signal (0-0.7 v), used to control the color,(iv)Green (G): Analog signal (0-0.7 v), used to control the color and (v) Blue (B): Analog signal (0-0.7 v), used to control the color. Different colors can be generated by altering the analog levels of the three RGB signals. Based on the values of the signals R, G, B one of the eight color will be displayed on the monitor listed in figure3

R	G	B	Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Figure 3 Display Color Codes

H-Sync: The h-sync pulse is an active low pulse which indicates the end of one line display in the VGA Monitor. In a typical 640x480 display, the display consists of 480 lines. Each line consists of 640 pixels and a h-sync pulse should contain 640 pixels information which is to be displayed in one line. A hsync signal is classified into four regions namely (a) Pulse width (T_{pw}) (b) front porch (T_{fp}) (c) display time (T_{disp}) and (d) back porch (T_{bp}) One full period of the hsync signal divided into 4 regions:

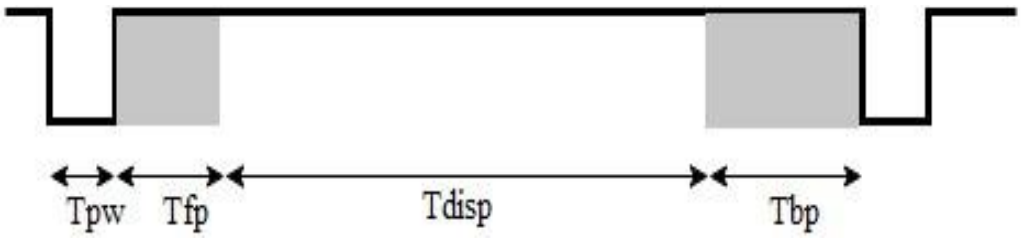

Figure 4 h-Sync Pulse

During the time T_{pw}, the electron beam returns to left edge, video signal is disabled and the h-sync and v-sync also found to be low. In T_{fp} duration the display portion of the monitor is not reached and the video signal is still disabled. The time of the signal in which pixel information is provided is displayed on the screen in the region T_{disp}. The time beyond which there is no display is termed as back porch time.

V-Sync: The v-sync pulse is also an active low pulse, indicating the end of one full frame. Inside display time of one v-sync pulse there will be 480 h-sync pulses. Similar to the h-sync pulse, v-sync pulse is also comprises of four regions namely Pulse width, front porch, display time and back porch.

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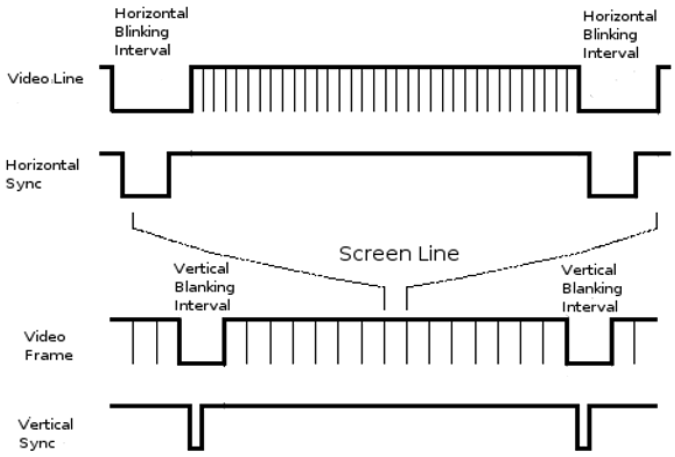

Figure 5 H-Sync AND V-Sync

III. RESULTS AND DISCUSSION

For implementing the VGA Controller different modules such as RGB, horizontal_Sync. Vertical_Sync, Clock has been obtained using Verilog programming in Xilinix ISE platform. RTL of each module is generated to verify the design. Testbenches has been created to validate the design through simulation waveform.

a. RTL Diagram of VGA

The RTL diagram of VGA is generated in Xilinx ISE tool after the synthesis. From the RTL diagram shown in figure 6 it can be clearly seen that the VGA controller consists of the horizontal sync, Vertical sync, RGB module and a clock module.

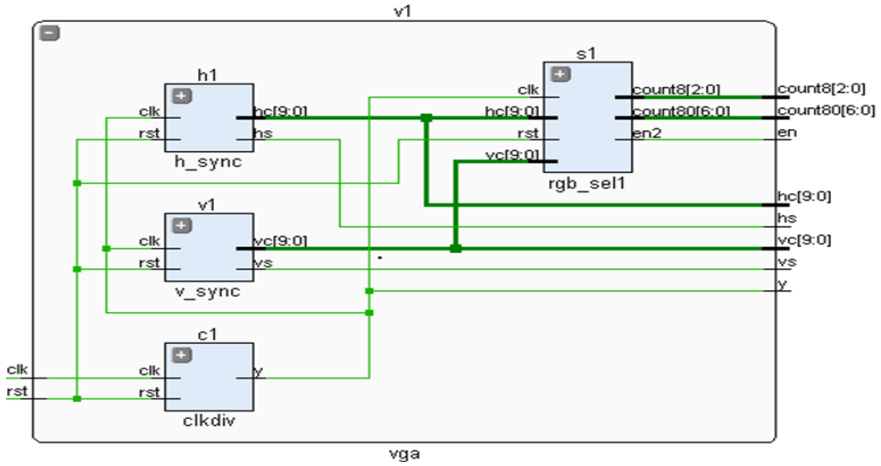

Figure 6 RTL Digaram of VGA Module

b. RTL Diagram of Horizontal Sync

Figure7.a and 7.b shows the RTL diagram for Horizontal Sync.

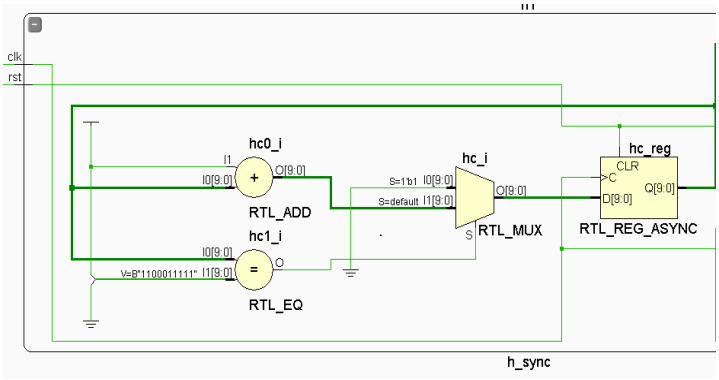

Figure 7.a RTL Digaram of Horizontal Sync Module

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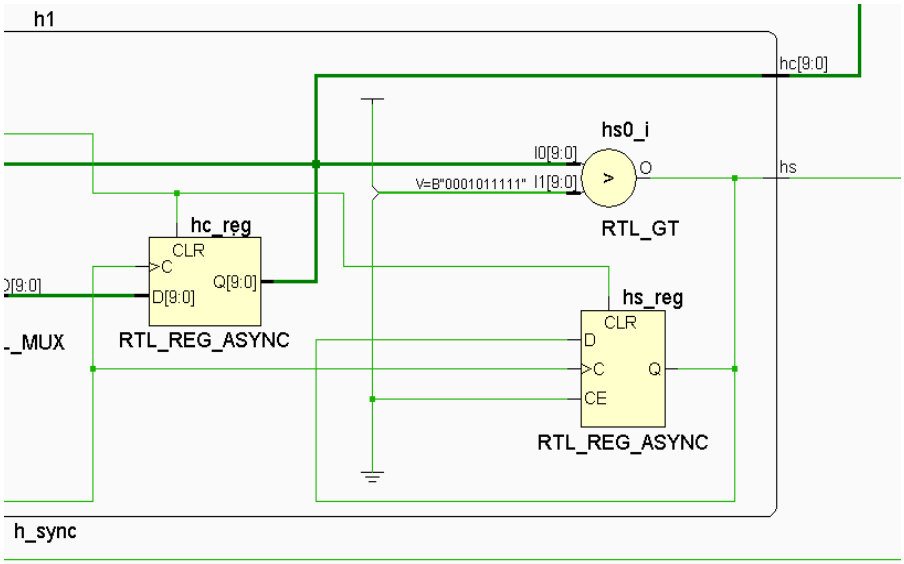

Fig.7.b RTL Digaram of Horizontal Sync Module

c. RTL Diagram of Vertical Sync

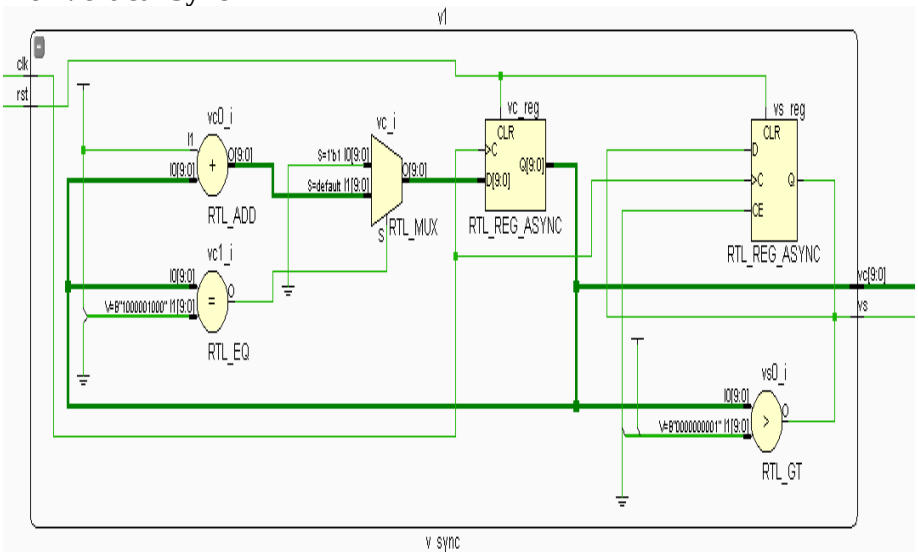

Fig.8 RTL Digaram of Vertical Sync Module

d. RTL Diagram of RGB

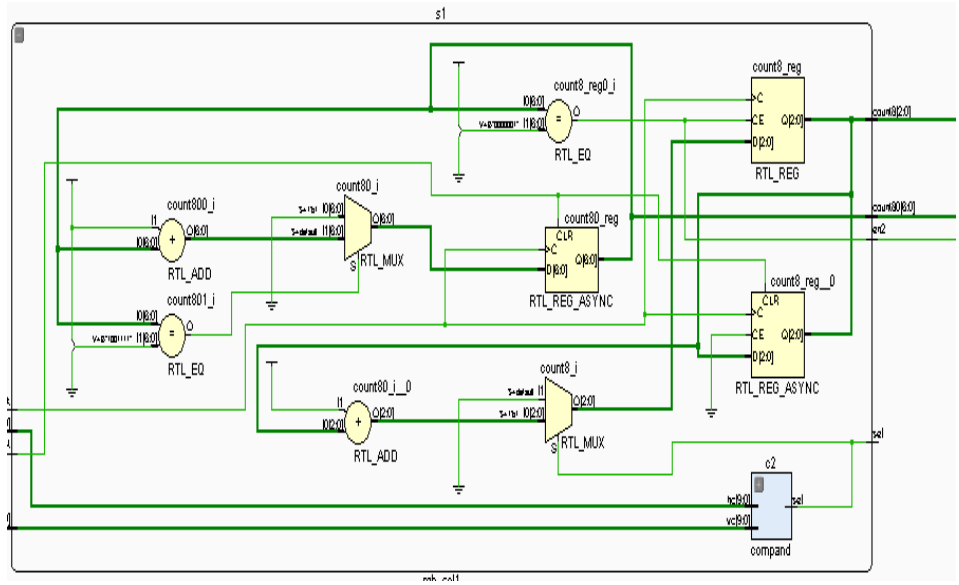

Figure 9 RTL Digaram of RGB Module

ISSN 2394 - 9554

e. RTL Diagram of Compand:

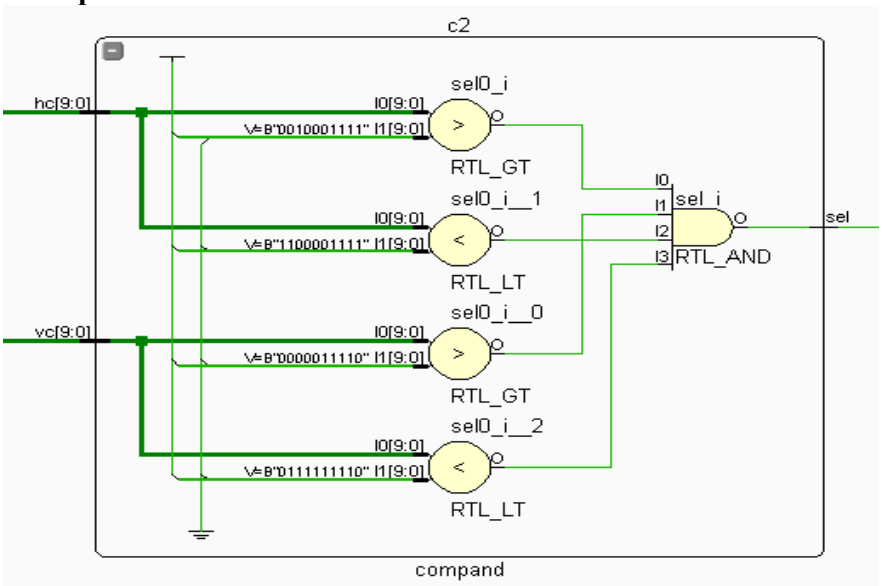

Figure 10 RTL Digaram of Compand Module

f. Simulation Waveform:

To validate the design of VGA controller different inputs are applied through testbench and simulation waveforms are obtained.

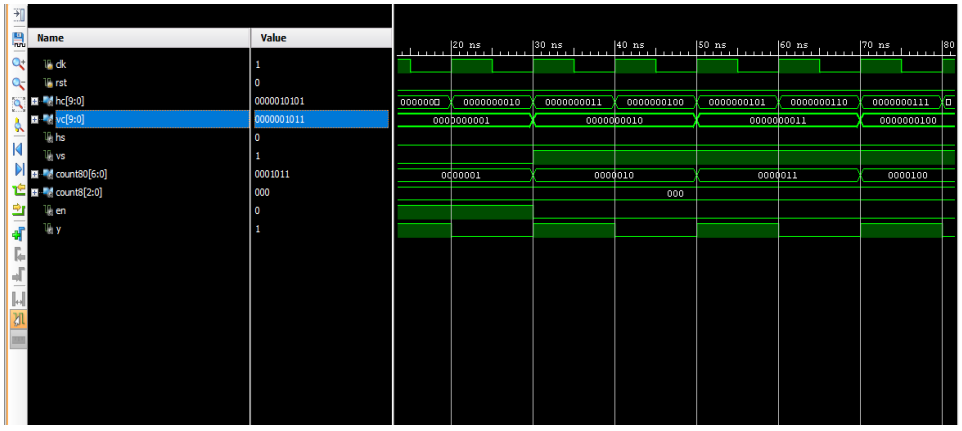

Figure 11 Simulation Waveform with Vs=1 and Hs=0

From the simulation waveform output shown in figure11 and 12 it can be noted that the controller generates the time sequence with respect to the horizontal sequence and vertical sequence set values. Using the time sequence different color bars are generated when its implemented with FPGA. The following figure shows the resultant color bars that is generated with respect to the generated time sequence and horizontal sequence set values

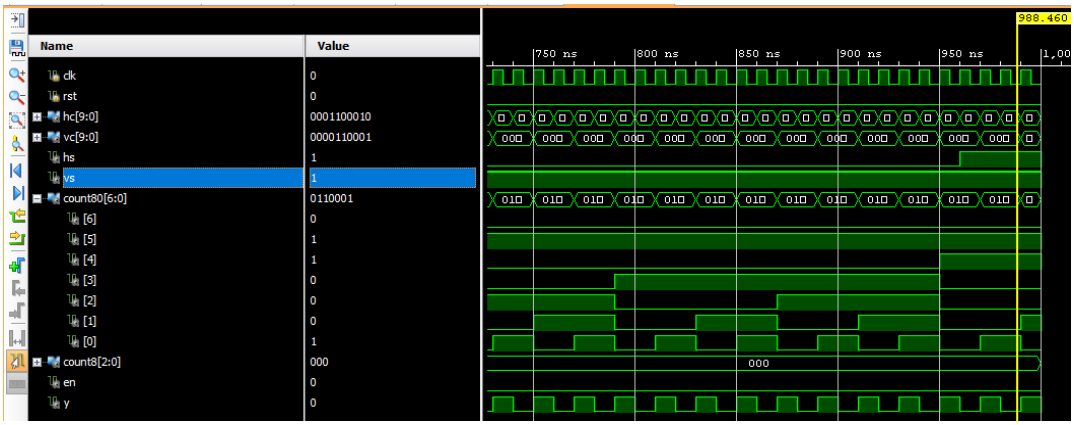

Figure 12 Simulation Waveform with Vs=0 and Hs=1

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Figure13 shows the resultant color bars that is generated with respect to the generated time sequence and horizontal sequence set values when connected to display monitor using FPGA implementation

Figure 13 Resultant Color Bar in Response to Timing, Hsync and Vsync

IV. CONCLUSION

In this paper Video Graphic Array which is a standard interface VGA which is used in different application such as surveillance systems, ATM machines, and video conferencing is presented. The model is designed using Verilog hardware description language. The code is synthesized netlist is obtained in the form of bit stream which is finally implemented in FPGA. Rigorous simulation studies are performed in order to validate the design.

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